BUILT IN SELF HEATING THERMAL TESTING OF FPGAs.

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OUTLINE.

1. INTRODUCTION.
2. EXISTING SYSTEM.
3. PROPOSED SYSTEM.
   - 3.1 BLOCK DIAGRAM.
   - 3.2 SELF HEATING CHAIN.
   - 3.3 SHE INTEGRATION WITH BIST.
4. RESULTS.
   - 4.1 SIMULATION RESULTS.
   - 4.2 RTL SCHEMATICS.
   - 4.3 DEVICE UTILISATION SUMMARY.
5. ADVANTAGES.
6. DISADVANTAGES.
7. FUTURE SCOPE.
8. COCLUSION.
9. REFERENCES.

1.INTRODUCTION.

- A Built In Self Test or Built In Test is a mechanism that Permits a machine to test itself.
- A thermal-aware testing of FPGAs using built-in self-heating.
- The internal logic resources of FPGA are used to build controlled self-heating elements (SHEs).
- Controlled SHE's are integrated with the test schemes.
- Two categories of SHE integration are there, they are
  1.BIST in application independent testing.
  2.self heating application dependent testing.

2. EXISTING SYSTEM.

2.1. BURN IN TESTING.

- The chip is exposed to high temperatures and/or voltages for certain periods.
- Accelerate the aging and stress of the chip before applying the test.
- External devices are used for heating up the chip.

2.2.THERMAL AWARE METHODS.

- The chip is first heated to a certain temperature and then the test is applied.
- External devices such as thermal chambers and ovens are used for the purpose of heating up the chip.

3.PROPOSED SYSTEM.

- Utilizing the idea of self heating.
- Make the FPGA able to generate heat by increasing the power consumption.

  3.1.BLOCK DIAGRAM.
- The basic block diagram of the BIST is depicted in figure 3.1.1.
- Consist of -

  1.Test pattern generator.

  2.Block under test.

  3.Output response analyzer.

  4.Test controller.

BLOCK DIAGRAM

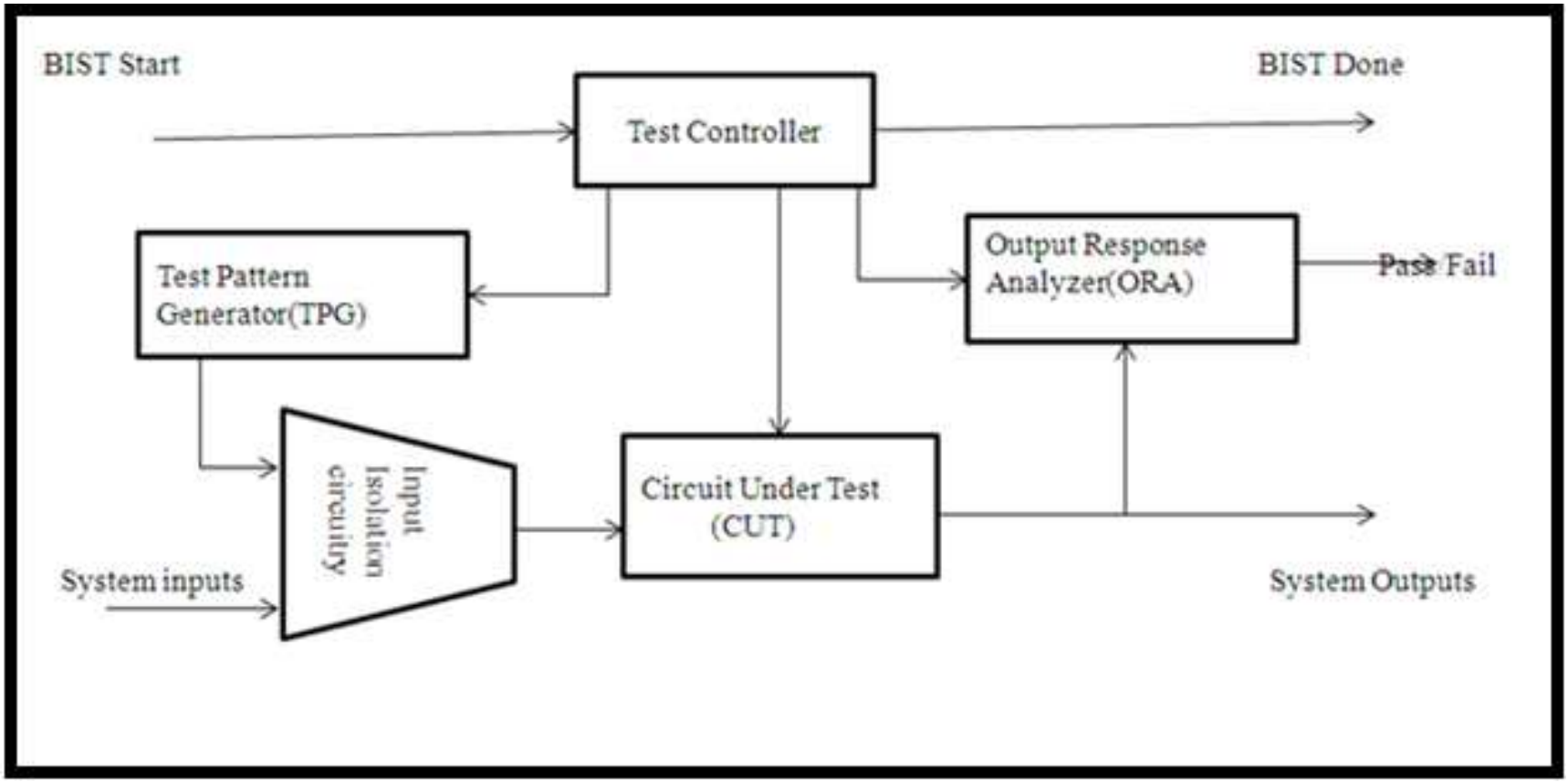

fig:3.1.1.BIST

BIST consists of several blocks as shown above.

- a) Test pattern Generator(TPG) : This is a circuit to be tested, a way to compress those results and way to analyze them.
  -It generates the test patterns for CUT. Here a Linear feedback shift register is used to generate patterns.
  -Patterns are generated in pseudo random fashion.
- b) Circuit under test(CUT) : The portion of the circuit tested in BIST mode. It can be combinational, sequential or a memory.
- c) Output Response Analyzer: It acts as a comparator with stored responses.
  -Compares the test output with the stored response and shows whether the chip passes or fails the test.
- d) Test controller: It controls the test execution.
  - It provides the control signal to activate all blocks.
  - If control signal is 0,then BIST is said to be in test mode and if 1,in normal mode.

3.2.SELF HEATING CHAIN.

- SHC controls the heat generated in the FPGA.
- Consist of a number of self heating elements.
- A Self heating element is depicted in figure 3.2.1.
- Consist of control circuit and toggle LUT'S.

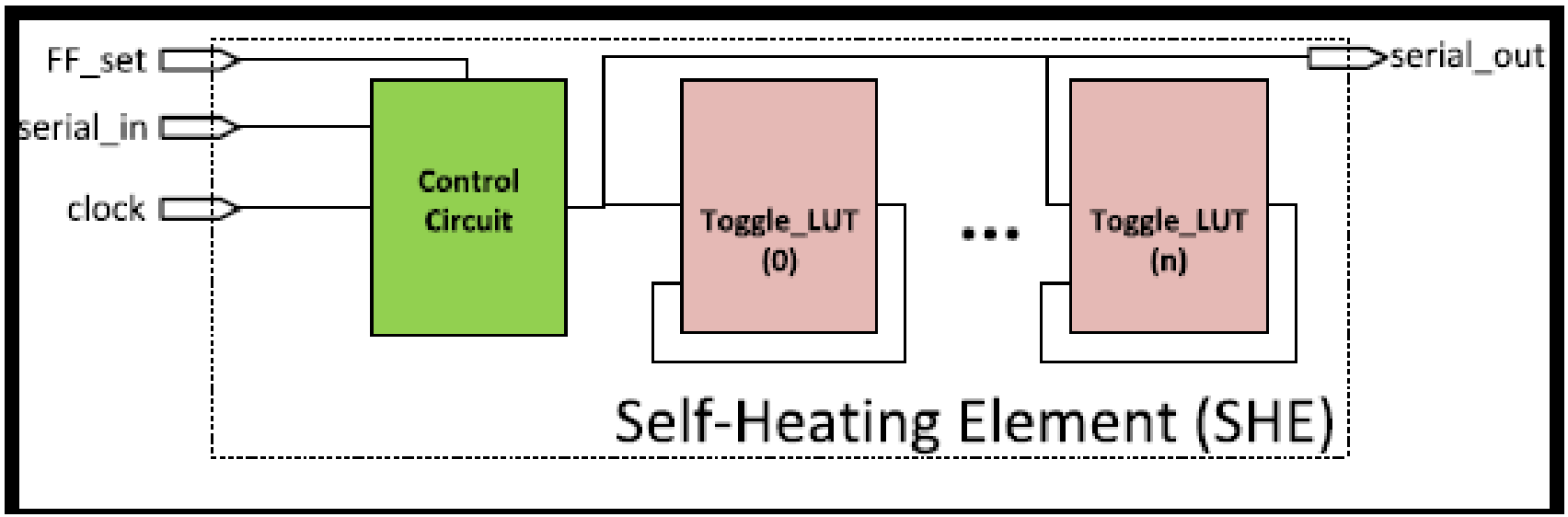

fig:3.2.1.SHE

- Basic toggle logic is depicted in figure 3.2.2.
- The circuit can be realized using an LUT with at least two inputs.
- The feedback signal from the LUT output to its input goes through switching resources.
- Causes the resources to toggle as well and hence their dynamic power consumption will increase.
- Thus enabling more heat to be generated.
- The Toggle LUT circuit is depicted in figure 3.2.3.
- To maximize the power consumption, each of the proposed SHEs consists of several toggling LUTs.

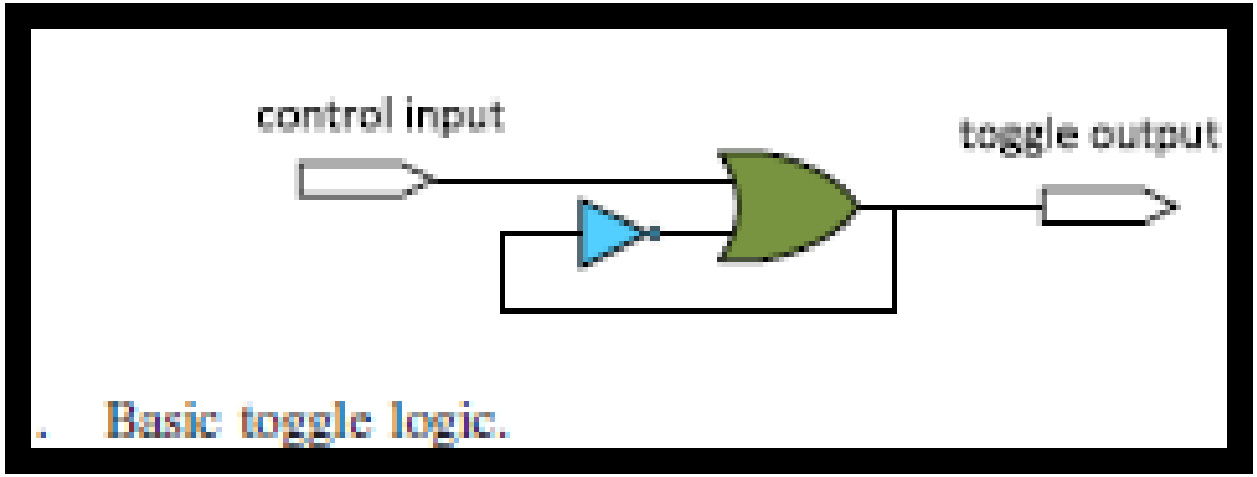

fig:3.2.2.BASIC TOGGLE

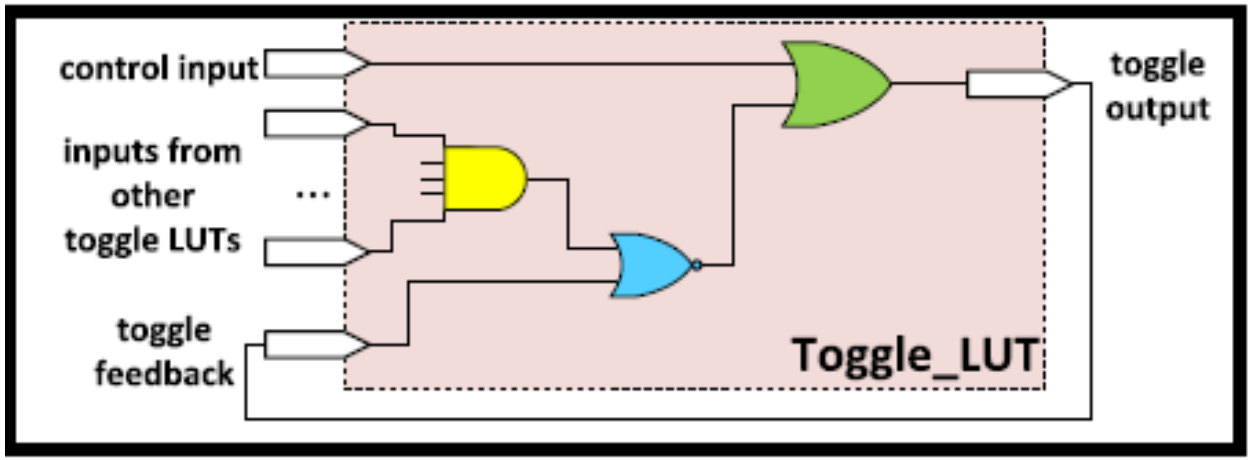

fig:3.2.3.TOGGLE LUT

- The control circuit sends serial out signal to the control input ports of toggling LUT'S.
- The control circuit of SHE is depicted in figure 3.2.4.
- Consist of flip flop working as a shift register.

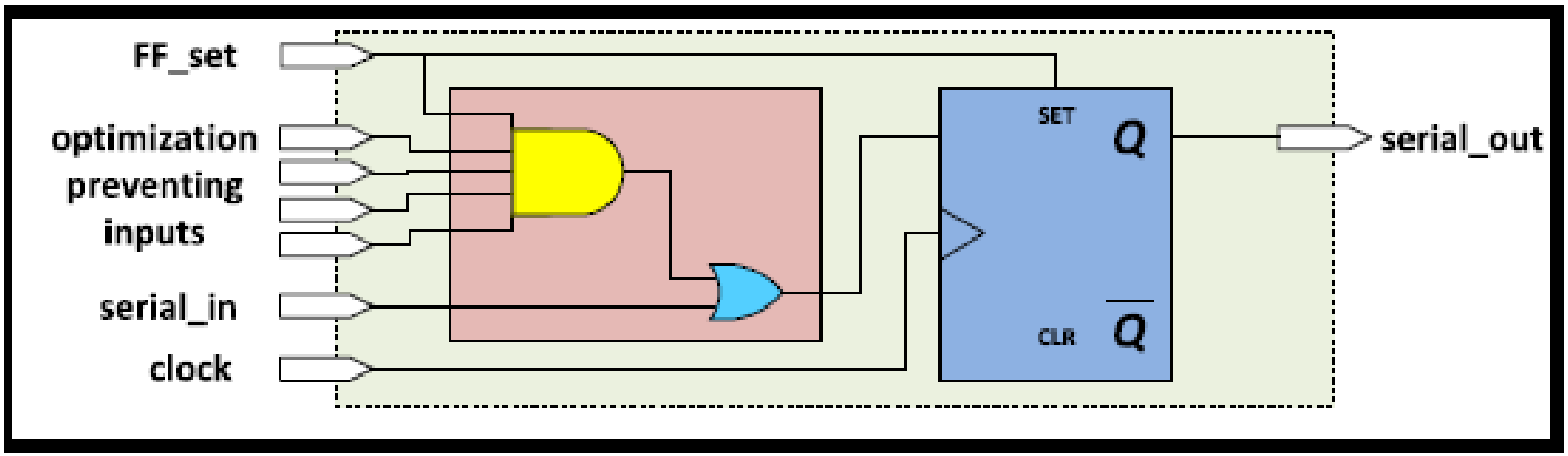

fig:3.2.4.CONTROL CIRCUIT

- In a single SHE, all of the toggling LUTs can be either in toggling mode or stopped, all at the same time.
- If SHE contains too many LUTs, a fine control of the generated temperature cannot be achieved.
- The serial-in and serial-out ports of multiple SHE's are connected together.
- Thus a SHE chain is developed.
- The SHE chain is depicted in the figure 3.2.5.
- Consist of a heating control input,clock and reset.

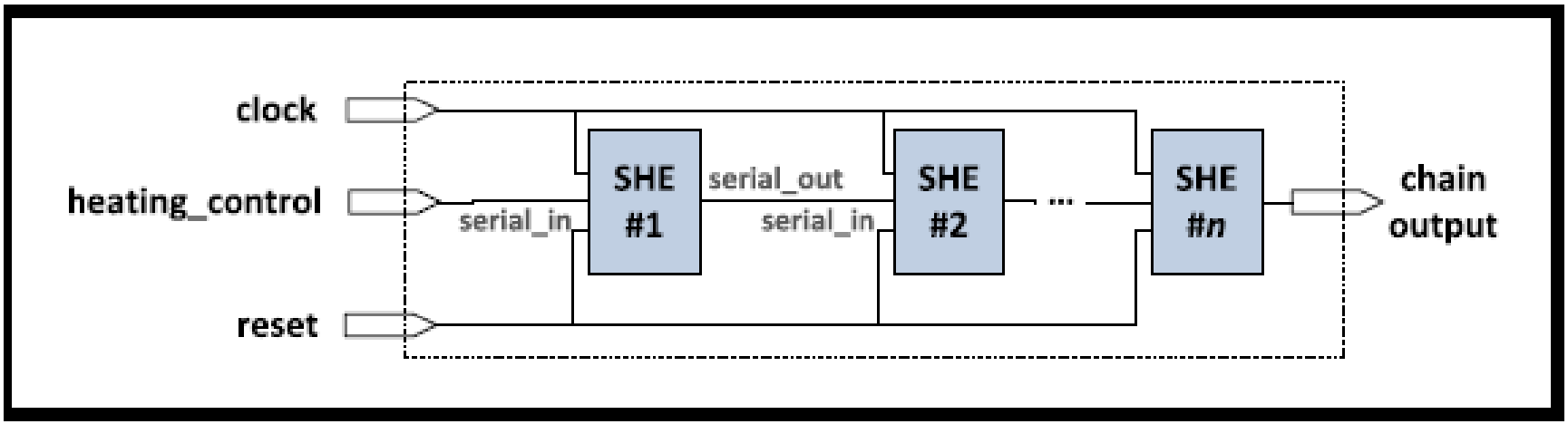

fig:3.2.5.SHE CHAIN

3.3.SHE INTEGRATION WITH BIST.

Two methods of integration of self heating with BIST are-

- Sequential methods.
  -FPGA's are loaded with SHE for heating up the chip in multiple heat and test configuration.
  -no need to modify original BIST structure.
- Concurrent methods.
  -FPGA's are loaded with SHE for heating up the chip in single heat and test configuration.
  -Original BIST structure is modified in order to free up enough logic resources for SHE.
  -Most commonly adopted technique.

4.1. SIMULATION RESULTS.

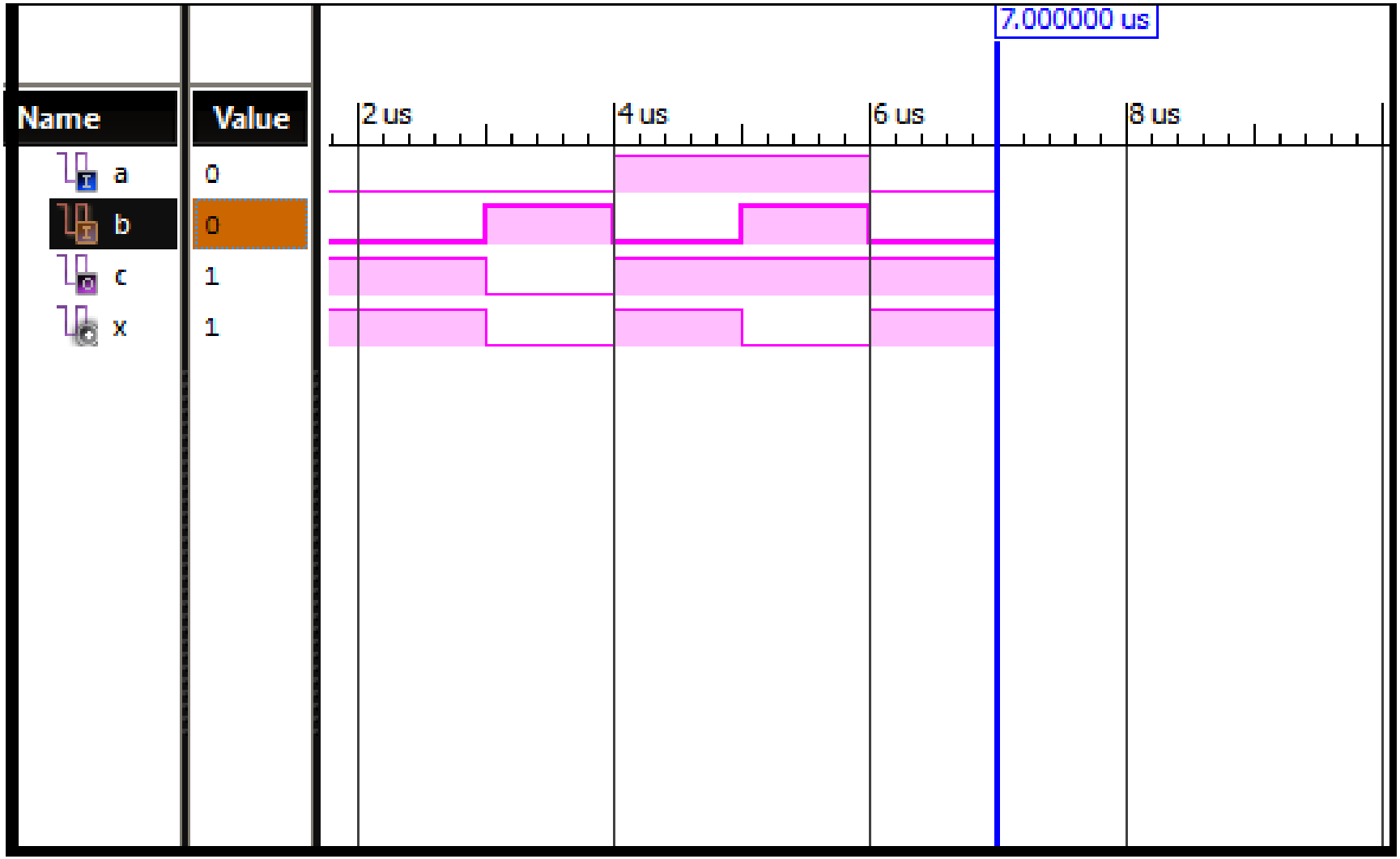

fig:4.1.1.BASIC TOGGLE SIMULATION

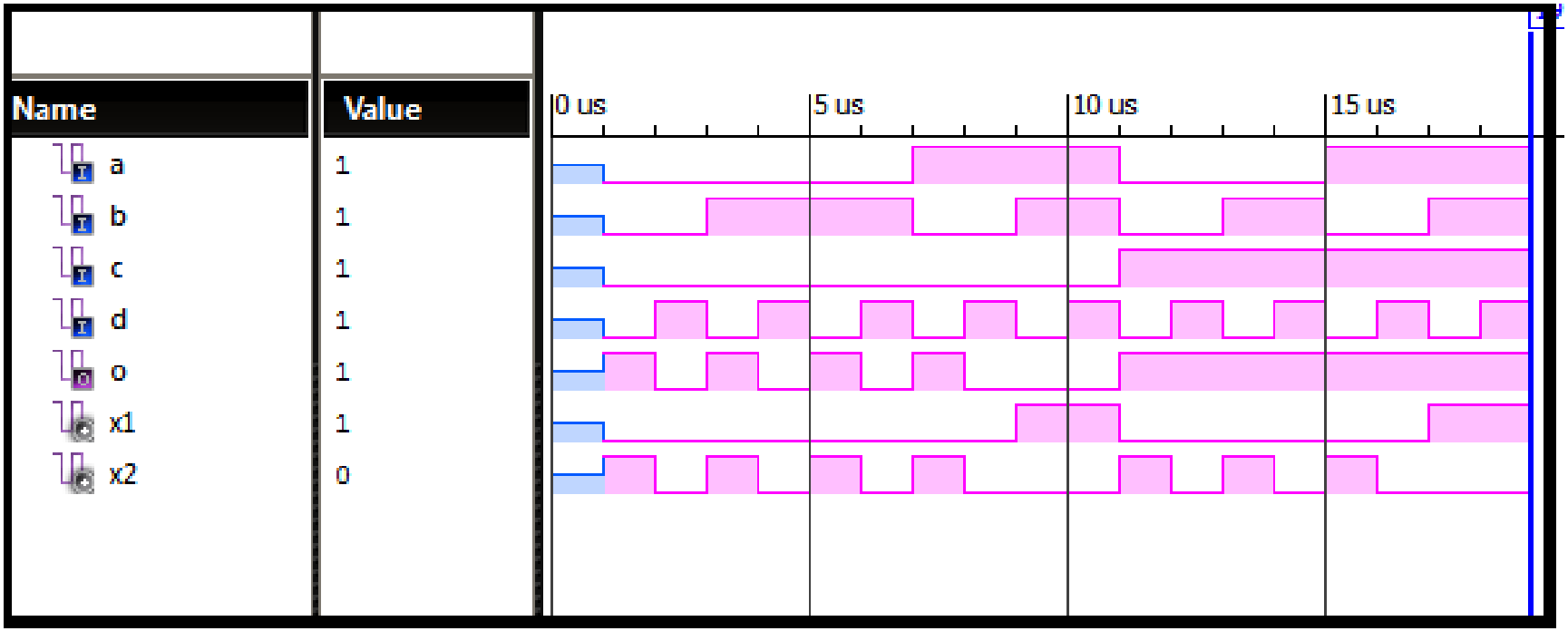

fig:4.1.2.TOGGLE LUT SIMULATION

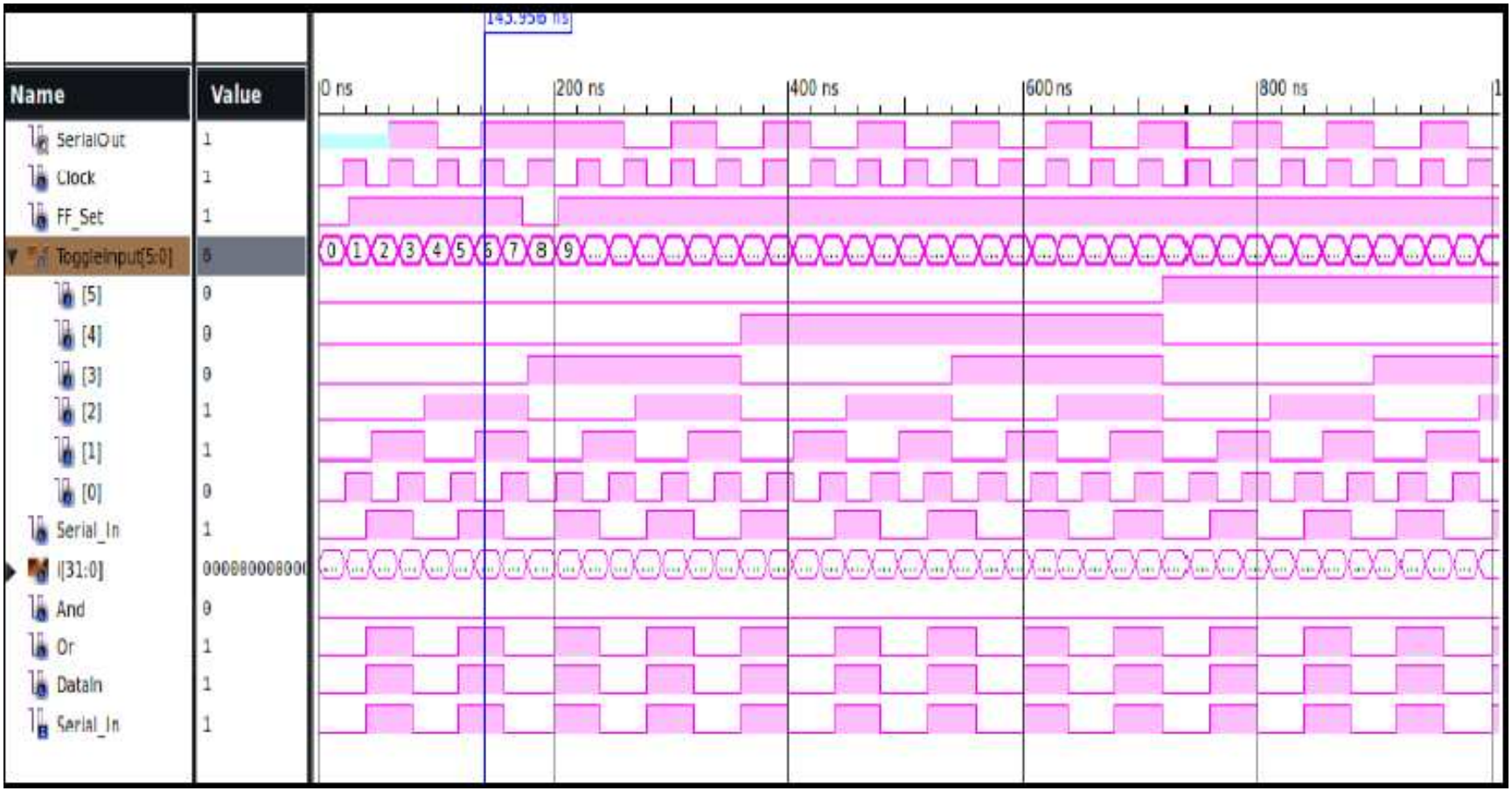

fig:4.1.1.SHE SIMULATION

4.2.RTL SCHEMATIC.

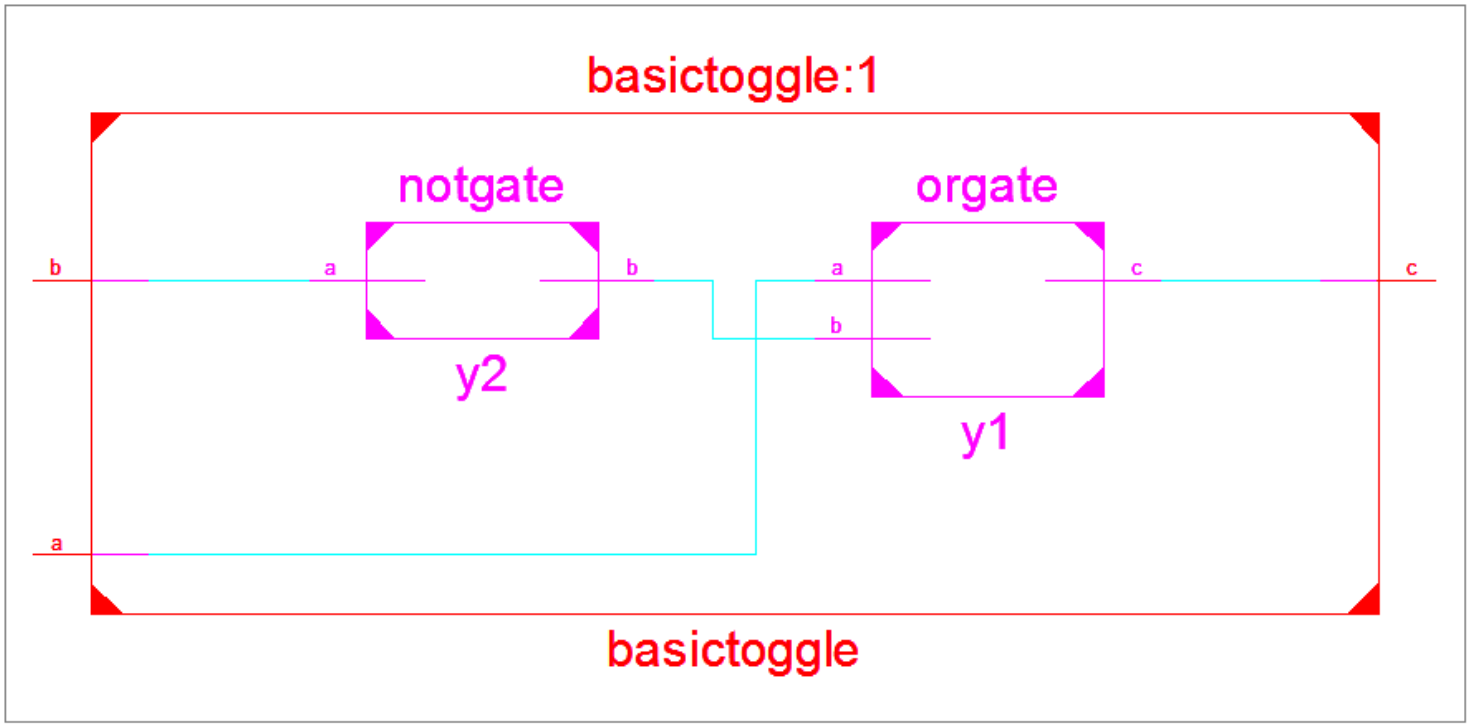

fig:4.2.1.BASIC TOGGLE RTL

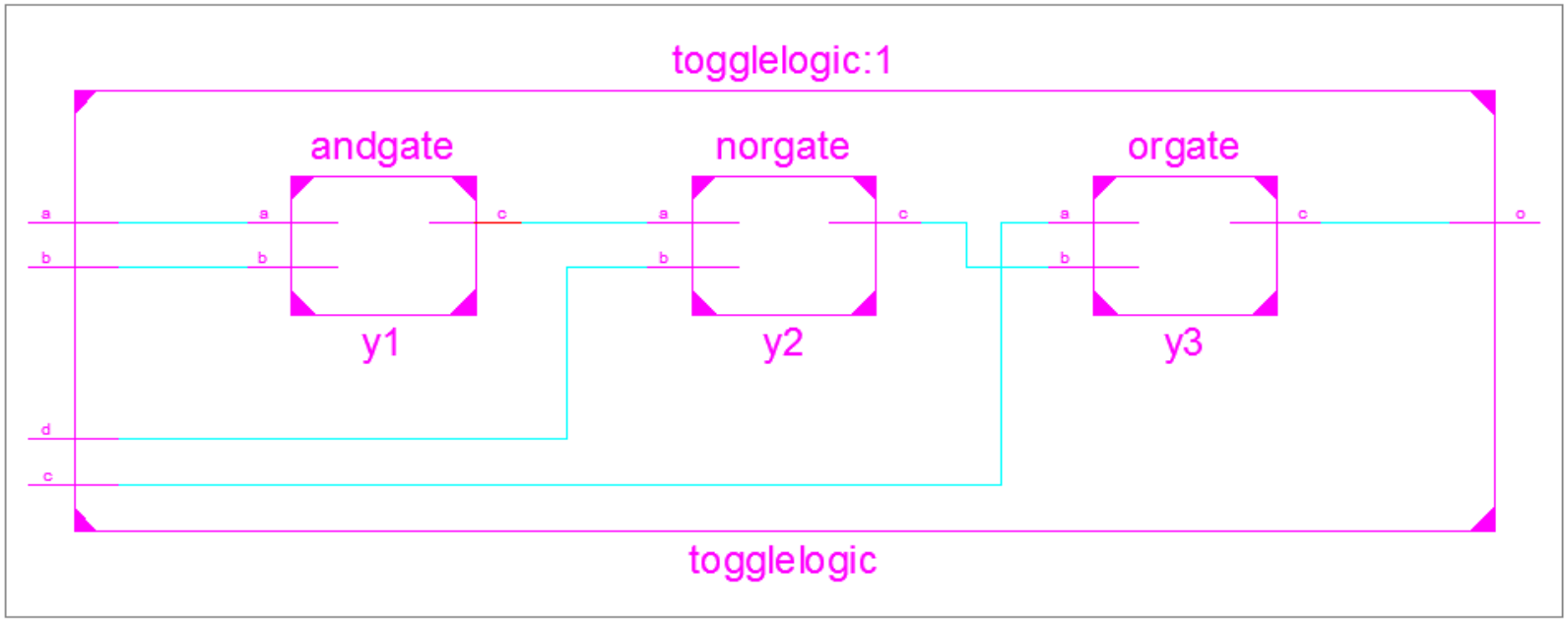

fig:4.2.2.TOGGLE LUT RTL

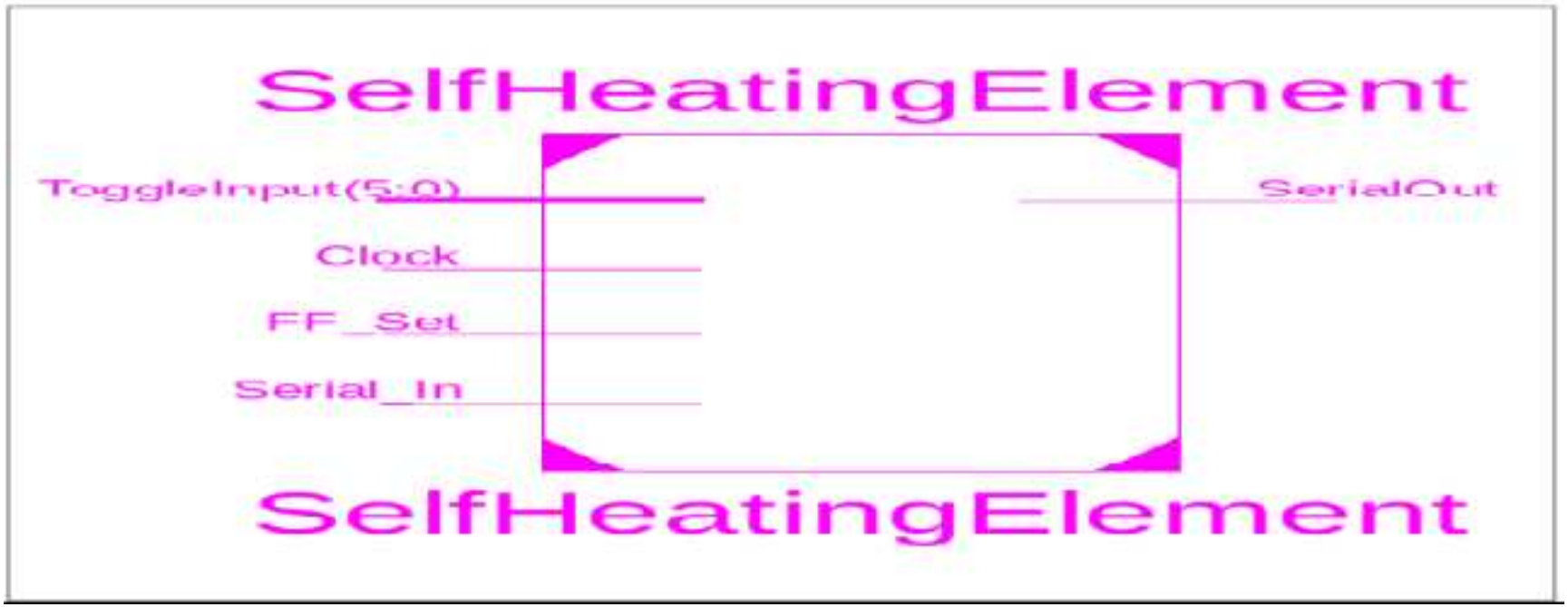

fig:4.2.3.SHE RTL

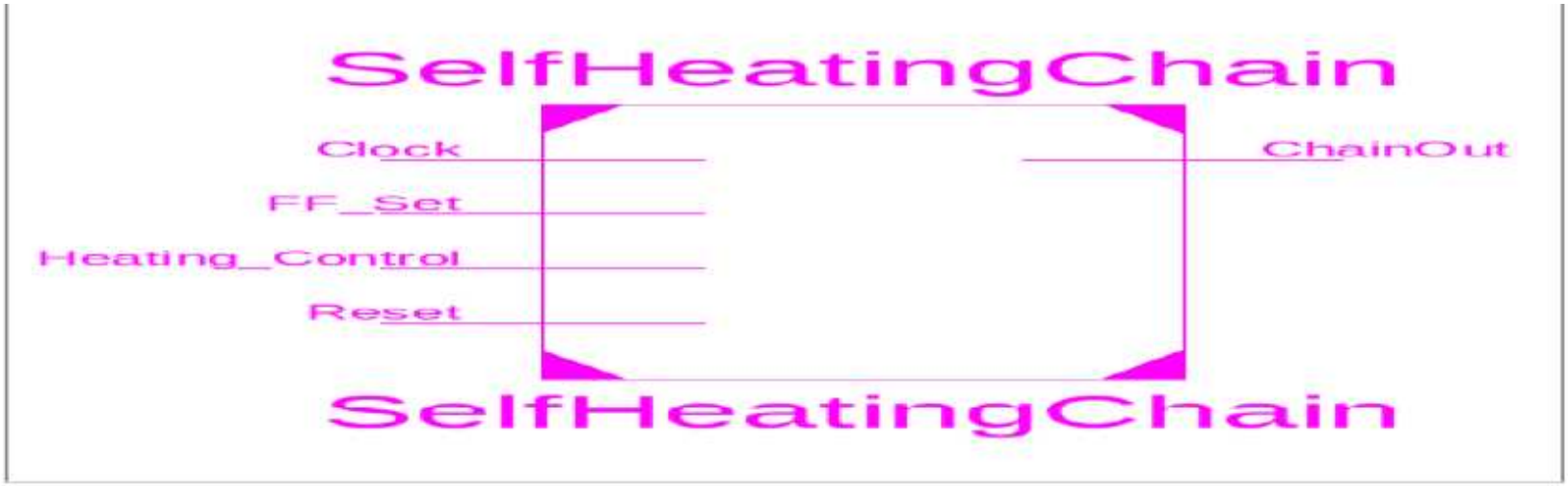

fig:4.2.4.SHE CHAIN RTL

4.3.DEVICE UTILIZATION SUMMARY.

-	Basictoggle	ToggleLUT	Controlckt	SHE
No: of LUTS	1/63400	1/63400	1/63400	1/63400
LUT Flip flop pairs	1	1	1	1
Number of I/o	3	5	5	8
delay	0.753ns	0.834ns	0.834ns	0.983ns

5.ADVANTAGES.

- Eliminates the need of any external device.
- Reducing the test cost and test time.
- Assuring heating only the FPGA chip and not any other component on the board.
- Generate uniform temperature on the chip.
- No limitation on the number of FPGA chips to be heated in parallel.

6.DISADVANTAGES.

- Performance penalty due to larger signal routing path in BIST.
- Area overheads.

7.FUTURE SCOPE.

- Utilized for real time applications such as FPGA implementation of BIST enabled UART.
- A restartable BIST controller for fault detection of FPGA can be possible.

8.CONCLUSION.

- Increasing chip temperature is one of the most important challenges that face chips at nano-scale.
- various failure mechanisms are accelerated at high chip temperature, which require thermal-aware testing to detect them.
- Thus a self heating approach for thermal-aware testing of FPGA devices is implemented.
- Upon simulation high accuracy is achieved.

9.REFERENCES.

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